BR1002 Datasheet

June 8, 2021

Version 1.1

Version History

Revision	Amendment	Date	Author
1.0	Initial version	2021-03-10	Yongqiang Xu
1.1	Modify the kernel	2021-06-08	BaoQiang Huang

Contents

Description

BR1002 is a power-optimized true system-on-chip (SoC) solution for both Bluetooth low energy and proprietary 2.4-GHz applications. It integrates a high performance and low power RF transceiver with Bluetooth baseband and rich peripheral IO extension. BR1002 also integrates a power management to provide high-efficient power management. It targets 2.4-GHz Bluetooth low energy systems, proprietary 2.4-GHz systems, Human-Interface Devices (keyboard, mouse, and remote control), sports and leisure equipment, mobile phone accessories and consumer electronics.

Processor

- 32bit RISC MCU, max 64MHz
- Dedicated Link Layer Processor
- Supports Over-The-Air Upgrade (OTA)
- SWD software upgrade
- Support debug mode

Power Management

- Supply voltage range 1.8V~3.6V
- 5.3mApeak current in RX
- 5.2mApeak current in TX (0dBm)
- 0.4uAin Hibernation mode without RTC clock
- 0.8uAin Hibernation mode with RTC clock
- 2.5uAin deep sleep mode
- Integrated DCDC BUCK Converter

Software

- Full compliant with BLE version 5.1, complete power-optimized stack, including controller and host
- Supports BT mesh network
- Support BLE sample applications and profiles
- Support HCI controller interface
- Support 6 Low PAN

Memory

- 64KB SRAM
- 48KB ROM
- 4Mbs sflash

Clocks

- 32.768K crystal oscillator clock, 32.768K RC clock
- 32M crystal oscillator clock, 32M RC clock

Peripherals

- 8 channels DMA
- UART x 2
- I2S interface
- Flexible General Purpose IOs, 17 general-purpose I/O GPIOs (max)
- I2C (master or slave) x 3
- SPI (master or slave) x 2
- One dedicated two-wire SPI LCD controller
- Watchdog to prevent system dead lock
- RTC
- Timers(32bit) x 3
- PWM 3 x 4
- Keyboard controller
- Three way QDEC
- Flexible GP-ADC: 6 single-end or differential-end 12bits GP-ADC
- Audio 16-bit ADC，SNR 93dB
- Touch sensor controller
- Fully programmable pin assignment
- AES HW encryption
- HW Random Number Generator

RF transceiver

- -95dBm sensitivity @1Mbps

- -93dBm sensitivity @2Mbps
- -96dBm sensitivity @500Kbps
- -100dBm sensitivity @125Kbps
- TX power -20~7dBm
- RSSI (1db resolution)

Package:

- 32-pin 4x4mm QFN32
- Completely RoHS-compliant

Application

- Home and Building Automation
- Connected Appliances, Lighting, Locks, Gateways, Security Systems
- Industrial
- Logistics, Production and Manufacturing, Automation, Asset Tracking and Management, Remote Display, Cable Replacement, HMI, Access Control
- Retail
- Beacons, Advertising, ESL and Price Tags, Point of Sales and Payment Systems
- Health and Medical
- Thermometers, Blood Glucose and Pressure Meters, Weight Scales, Vitals Monitoring, Hearing Aids
- Sports and Fitness
- Activity Monitors and Fitness Trackers, Heart Rate Monitors, Running Sensors, Biking Sensors, Sports Watches, Gym Equipment, Team Sports Equipment
- GATT and HID over GATT
- Remote Controls, Keyboards and Mice, Gaming
- Accessories
- Toys, Trackers, Luggage Tags, Wearables

1. Block Diagram

BR1002 supports user secondary development and provides a simpler interface. it integrates Bluetooth baseband, PHY and proprietary 2.4GHz protocol and profiles (GATT master and slave, HID over GATT). BR1002 accesses system hardware resource by AHB bus, ROM, RAM, DMA, SFLASH, GPIO exchange data through AHB bus, and all other peripheral is accessed through AHB to APB Bridge and APB bus.

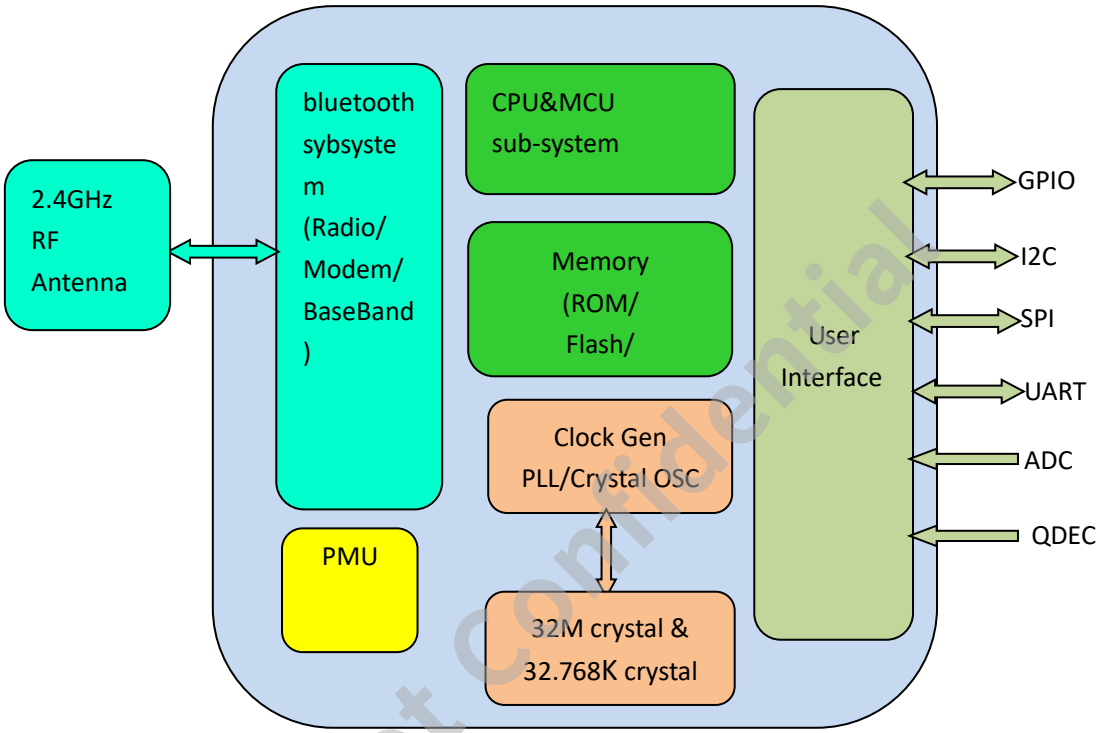

Figure 1 BR1002 Functional Diagram

2. PIN Description

2.1. PIN Diagram

BR1002's size is 32-pin 4x4mm QFN32 package. Figure 2 shows the QFN32 pin definition. BR1002 have GND PAD in the center.

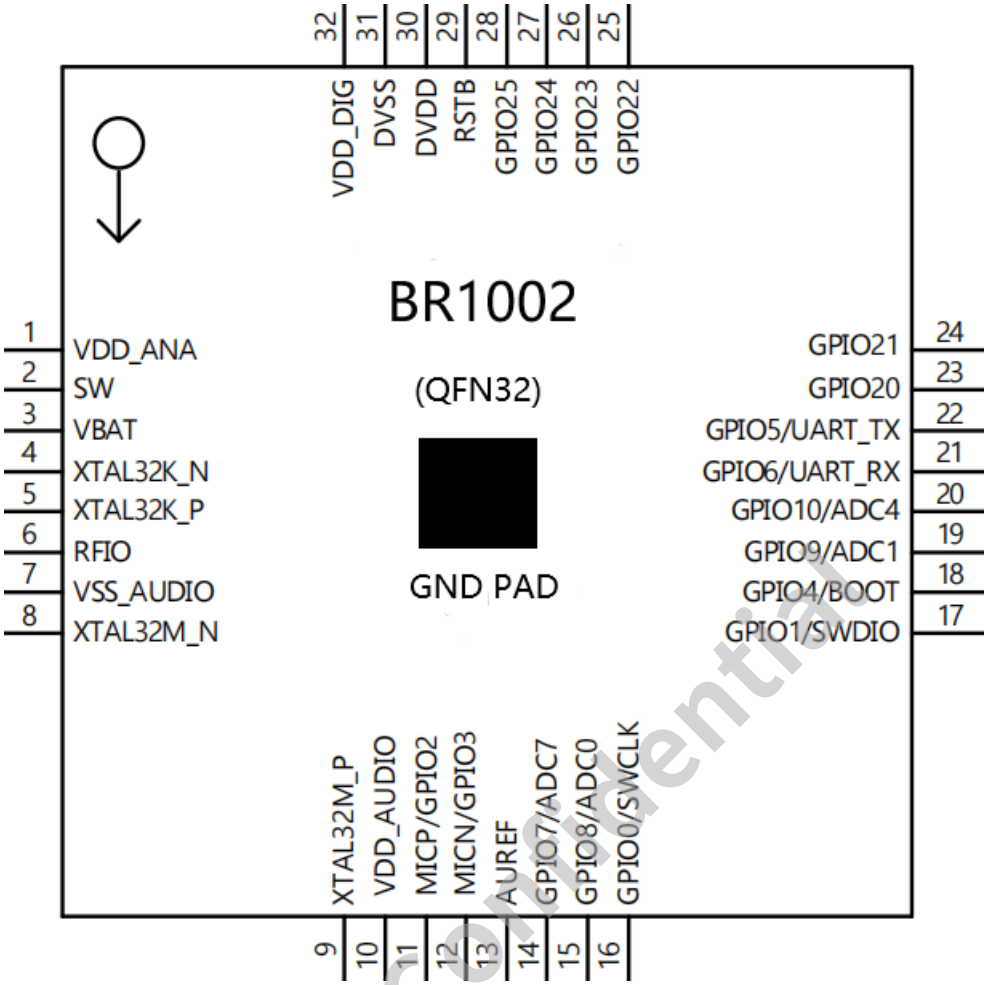

Figure 2 BR1002 PIN Top View

2.2. PIN Definition

Table 1 PIN Definition

No.	Name	Type	Description
1	VDD_ANA	Power	DCDC output to analog
2	SW	Power	DCDC output connected with external devices
3	VBAT	Power	Power supply 1.8V~3.6V
4	XTAL32K_N	Analog	32K crystal oscillator N input
5	XTAL32K_P	Analog	32K crystal oscillator P input
6	RFIO	Analog	RF input/output
7	VSS_AUDIO	Power	Audio ground
8	XTAL32M_N	Analog	32M crystal oscillator N input
9	XTAL32M_P	Analog	32M crystal oscillator P input
10	VDD_AUDIO	Power	MIC Bias
11	MICP/GPIO2	Analog/Digital	MICP input and Digital GPIO
12	MICN/GPIO3	Analog/Digital	MICN input and

			Digital GPIO
13	AUREF	Analog	AUDIO ADC Reference
14	GPIO7/ADC7	Digital /Analog	Digital and Analog GPIO
15	GPIO8/ADC0	Digital/Analog	Digital and Analog GPIO
16	GPIO0/SWCLK	Digital	Digital GPIO
17	GPIO1/SWDIO	Digital	Digital GPIO
18	GPIO4/BOOT	Digital	Digital GPIO
19	GPIO9/ADC1	Digital/Analog	Digital and Analog GPIO
20	GPIO10/ADC4	Digital/Analog	Digital and Analog GPIO
21	GPIO6/UART_RX	Digital	Digital GPIO
22	GPIO5/UART_TX	Digital	Digital GPIO
23	GPIO20	Digital/Analog	Digital and Analog GPIO
24	GPIO21	Digital/Analog	Digital and Analog GPIO
25	GPIO22	Digital/Analog	Digital and Analog GPIO
26	GPIO23	Digital/Analog	Digital and Analog GPIO
27	GPIO24	Digital/Analog	Digital and Analog GPIO
28	GPIO25	Digital/Analog	Digital and Analog GPIO
29	RSTB	Digital	Reset signal
30	DVDD	Power	Digital power
31	DVSS	Power	Digital ground
32	VDD_DIG	Power	DCDC output to digital

Note 1: All digital peripheral pins can be programmed to any GPIO

3. Electrical Characteristics

3.1. Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings

Parameter	Min	Max	Unit
Supply voltage (VBAT)	-0.3	3.9	V
Maximum Junction Temperature	-40	125	℃
Storage Temperature	-40	125	℃

3.2. Recommended Operating Conditions

Table 3 Recommended Operating Conditions

Parameter	Min	Typ.	Max	Unit
Operating temp	-40	-	85	℃
Digital Core supply voltage(DVDD)	0.9	1.0	1.2	V
Internal analog LDO power supply (VDD_ANA)	1.1	1.25	1.4	V

Internal digital LDO power supply (VDD_DIG)	1.1	1.25	1.4	V
I/O voltage	VBAT	VBAT	VBAT	V
Supply voltage(VBAT)	1.8	3.3	3.6	V

3.3. BLE RF Characteristics

3.3.1. Transmitter

Supply Voltage = 3.3V@25℃

Table 4 RF Transmitter Characteristics

Parameters	Min	Typ.	Max	Unit
Max RF transmit power	-	7	-	dBm
RF power control range	-20	-	7	dB
Δf 1avg maximum modulation (uncoded data at 1 Ms/s)	225	250	275	KHz
Δf 1avg maximum modulation (uncoded data at 2 Ms/s)	450	500	550	KHz
Δf 2max maximum modulation (uncoded data at 1 Ms/s)	100%	-	-	-
Δf 2max maximum modulation (uncoded data at 2 Ms/s)	100%	-	-	-
Δf 2max maximum modulation (LE Coded (S=8))	100%	-	-	-
Δf 2avg /Δf 1avg (uncoded data at 1 Ms/s)	0.84	-	-	-
Δf 2avg /Δf 1avg (uncoded data at 2 Ms/s)	0.84	-	-	-
Frequency Accuracy (uncoded data at 1 Ms/s)	-	4.03	-	Khz
Frequency Accuracy (uncoded data at 2 Ms/s)	-	9.08	-	KHz
Frequency Accuracy (LE Coded (S=8))	-	6.08	-	KHz
Frequency Offset (uncoded data at 1 Ms/s)	-	4.02	-	KHz
Frequency Offset (uncoded data at 2 Ms/s)	-	4.02	-	KHz
Frequency Offset (LE Coded (S=8))	-	4.02	-	KHz
Frequency Drift (uncoded data at 1 Ms/s)	-	-3.31	-	KHz
Frequency Drift (uncoded data at 2 Ms/s)	-	-3.31	-	KHz
Frequency Drift (LE Coded (S=8))	-	-3.31	-	KHz
Frequency Drift rate (uncoded data at 1 Ms/s)	-	-3.13	-	KHz/50uS
Frequency Drift rate (uncoded data at 2 Ms/s)	-	-3.13	-	KHz/50uS
Frequency Drift rate (LE Coded (S=8))	-	-3.13	-	KHz/50uS
Initial Frequency Drift (uncoded data at 1 Ms/s)	-	-2.25	-	KHz
Initial Frequency Drift (uncoded data at 2 Ms/s)	-	-2.25	-	KHz
Initial Frequency Drift (LE Coded (S=8))	-	-2.25	-	KHz
2nd harmonic content	-	-	-50	dBm
3rd harmonic content	-	-	-50	dBm

3.3.2. BLE Receiver

Supply Voltage = 3.3V@25℃

Table 5 BLE Receiver

Parameters		Min	Typ.	Max	Unit
Sensitivity, uncoded data at 1 Ms/s		-	-95	-	dBm
Sensitivity, uncoded data at 2 Ms/s		-	-93	-	dBm
Senstivity, LE Coded (S=2)		-	-96	-	dBm
Sensitibity, LE Coded (S=8)		-	-100	-	dBm
Maximum received signal , uncoded data at 1 Ms/s		-	-	-1.5	dBm
Maximum received signal , uncoded data at 2 Ms/s		-	-	-1.5	dBm
Maximum received signal , uncoded data at 500 Ks/s		-	-	-1.5	dBm
Maximum received signal , uncoded data at 125 Ks/s		-	-	-1.5	dBm
C/I co-channel Sensitivity, uncoded data at 1 Ms/s		-	-	3	dB
C/I co-channel Sensitivity, uncoded data at 2 Ms/s		-	-	2.6	dB
C/I co-channel Sensitivity, uncoded data at 500 Ks/s		-	-	1.2	dB
C/I co-channel Sensitivity, uncoded data at 125 Ks/s		-	-	0.5	dB
Adjacent channel selectivity C/I Note: F 0 =2440MHz	F = F0+1MHz , uncoded data at 1 Ms/s	-	-	-38	dB
	F = F0 -1MHz , uncoded data at 1 Ms/s	-	-	-17	dB
	F = F0+2MHz , uncoded data at 1 Ms/s	-	-	-41	dB
	F = F0-2MHz , uncoded data at 1 Ms/s	-	-	-19	dB
	F = F0+3MHz , uncoded data at 1 Ms/s	-	-	-45	dB
	F = F0-3MHz , uncoded data at 1 Ms/s	-	-	-42	dB
	F = F0+2MHz , uncoded data at 2 Ms/s	-	-	-39	dB
	F = F0-2MHz , uncoded data at 2 Ms/s	-	-	-17	dB
	F = F0+4MHz , uncoded data at 2 Ms/s	-	-	-43	dB
	F = F0-4MHz , uncoded data at 2 Ms/s	-	-	-32	dB
	F = F0+6MHz , uncoded data at 2 Ms/s	-	-	-46	dB
	F = F0-6MHz , uncoded data at 2 Ms/s	-	-	-42	dB
	F = F0+1MHz , uncoded data at 500 Ks/s	-	-	-38	dB

	F = F0 -1MHz , uncoded data at 500 Ks/s	-	-	-26	dB
	F = F0+2MHz , uncoded data at 500 Ks/s	-	-	-51	dB
	F = F0-2MHz , uncoded data at 500 Ks/s	-	-	-24	dB
	F = F0+3MHz , uncoded data at 500 Ks/s	-	-	-53	dB
	F = F0-3MHz , uncoded data at 500 Ks/s	-	-	-53	dB
	F = F0+1MHz , uncoded data at 125 Ks/s	-	-	-36	dB
	F = F0 -1MHz , uncoded data at 125 Ks/s	-	-	-31	dB
	F = F0+2MHz , uncoded data at 125 Ks/s	-	-	-53	dB
	F = F0-2MHz , uncoded data at 125Ks/s	-	-	-29	dB
	F = F0+3MHz , uncoded data at 125 Ks/s	-	-	-57	dB
	F = F0-3MHz , uncoded data at 125 Ks/s	-	-	-55	dB

3.4. Power Consumption

Table 6 Chipset Power Consumption (VBAT=3.3V)

Operation Modes	LDO	DCDC	Unit
Chip deep sleep	0.4	0.4	uA
Chip active	3.2	1.5	mA
Peak of Bluetooth transfer (0dBm)	11.5	5.2	mA
Peak of Bluetooth receiver	12.1	5.3	mA

4. Functions Description

4.1. RF Transceiver

The Radio Transceiver implements the RF part of the Bluetooth Low Energy protocol. Together with the Bluetooth 5.1 PHY layer, this provides a reliable wireless communication. All RF blocks are supplied by on-chip low-drop out-regulators (LDO's). The Bluetooth LE radio comprises the Receiver, Transmitter, Synthesizer, Rx/Tx combiner block, and Biasing LDO's.

4.2. RF Receiver

The BR1002 receiver is a low IF down conversion architecture. The RF signal passes first through an integrated transformer, which is shared between receiver and transmitter. The transformer drives a differential variable-gain LNA, which amplifies the signal before it passes through a low-IF down conversion mixer stage.
Following the mixer is a third-order complex BPF, which performs channel selection and image rejection. The IF signal is then digitized by two noise-shaping SAR ADCs before further signal processing in the digital domain.

4.3. RF Transmitter

The BR1002 transmitter is a direct modulating architecture. The digital baseband signals directly modulate VCO and divider of PLL, which is called two-point modulation. After a 3-stage B-class power amplifier, the radio signal is output through antenna.

4.4. Frequency Synthesizer

The BR1002 Frequency synthesizer is fully integrated sigma delta fractional-N PLL to lock the VCO to a reference crystal oscillator. The synthesizer uses a number of integrated linear regulators for better isolation to the blocks respectively.

4.5. Bluetooth Baseband Unit

The BLE (Bluetooth Low Energy) core is a qualified Bluetooth 5.1 baseband controller compatible with Bluetooth Smart specification and it is in charge of packet encoding/decoding and frame scheduling.

Features:

- All device classes support (Broadcaster, Central, Observer, Peripheral)
- All packet types (Advertising / Data / Control)
- Encryption (AES / CCM)
- Bit stream processing (CRC, Whitening)
- Frequency Hopping calculation
- Low power modes supporting 32.768kHz

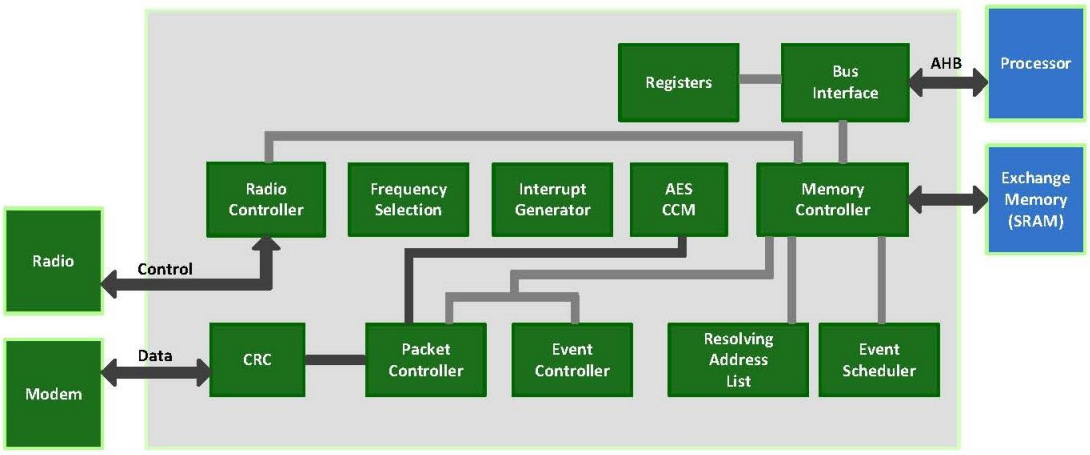

Figure 3 BR1002 Baseband

5. Interfaces Description

5.1. SPI

The Serial Peripheral Interface (SPI) bus is a synchronous serial communication interface specification used for short distance communication, primarily in embedded systems. The BR1002 integrate 2 SPI interfaces, they can work in either master or slave mode and also support DMA or software mode to transfer data. The master or slave controller only support point to point connection by hardware, that is, both the SPI interface has only one CS pin. The connection is shown below the figure.

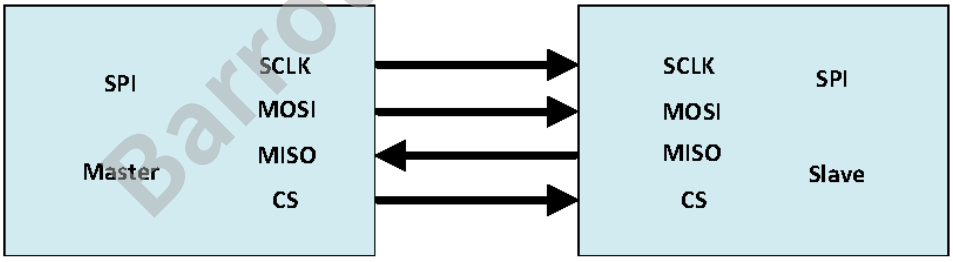

Figure 4 SPI Connection

The flexibility of SPI interface makes it suitable for most of SPI slave devices. SPI offers four modes due to the programmable ability of SCK's polarity and phase. The delay from CS to SCK, the delay from SCK to NCS and SCK period are also programmable. SPI interface timing diagram is shown in Figure5 below.

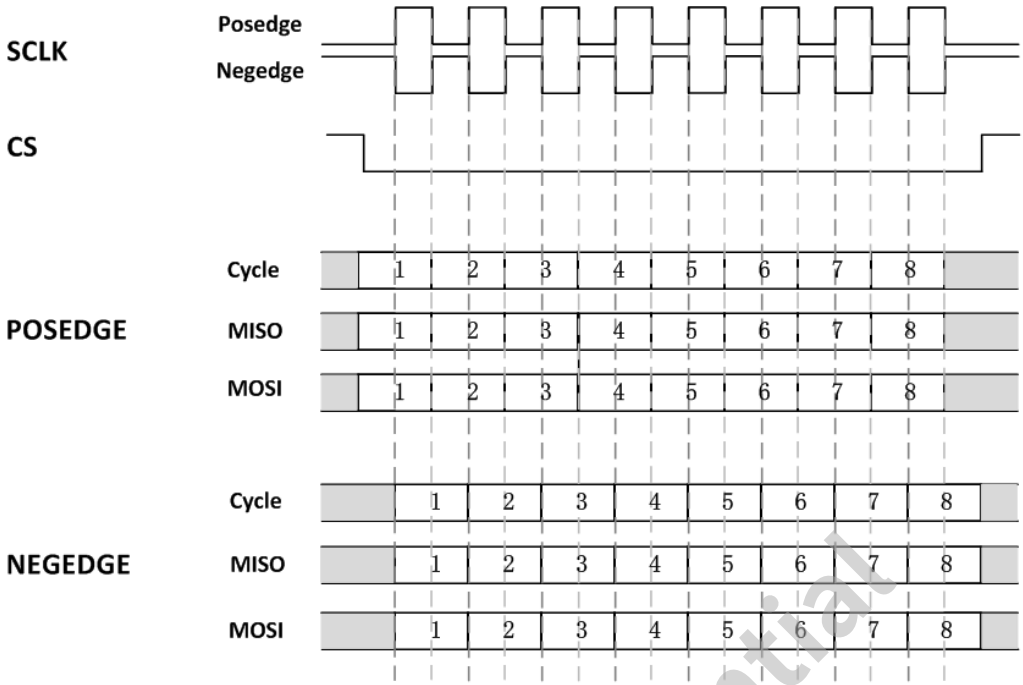

Figure 5 SPI Interface Timing Diagram

5.2. UART

The UART is modeled after the industry-standard 16550. However, the register address space has been relocated to 32-bit data boundaries for APB bus implementation.

The UART is used for serial communication with a peripheral, modem (data carrier equipment, DCE) or data set. Data is written from a master (CPU) over the APB bus to the UART and it is converted to serial form and transmitted to the destination device. Serial data is also received by the UART and stored for the master (CPU) to read back. The UART contains registers to control the character length, baud rate, parity generation/checking, and interrupt generation. Although there is only one interrupt output signal from the UART, there are several prioritized interrupt types that can be responsible for its assertion. Each of the interrupt types can be separately enabled or disabled by the control registers.

BR1002 has 2 UART; the UART0 is a common 2 wire (transmitter and receiver) controller, and the UART1 support stream control (CTS/RTS).

5.3. I2C

The I2C is a master or slave interface. It supports 100, 400 and 800 KHz clock rates for controlling EEPROM and etc. The I2C interface provides several data formats and can fit various I2C peripherals. Sequential read and write are supported to improve throughputs. The I2C support DMA operation for extra MCU free data transfer. The I2C work as either master or slave, but cannot change the working mode after configuration.

6. Timers

The Timer includes three identical 32-bit Timer Counter channels. Each channel can be independently programmed to perform a wide range of functions including frequency measurement, event counting, interval measurement, pulse generation, delay timing and pulse width modulation. Each channel drives an internal interrupt signal which can be programmed to generate processor interrupts.

7. GPIO

BR1002 has up to 17 software-configurable I/O pins.

- Fully programmable pin assignment;
- Selectable pull-up, pull-down resistors per pin;
- GPIO[2,3,7,8,9,10] ability to be configured as GP-ADC input;
- Pins retain their last state when system enters the sleep mode;
- Ability to wakeup chip by any GPIOs in sleep mode.

8. I2S

The I2S have three wires: serial data, word select and serial clock and this interface is used for audio data transfer. The BR1002 I2S interface supports both master and slave mode for transmitter and receiver. The I2S supports the standard I2S frame format.

9. Quadrature Decoders

This block decodes the pulse trains from a rotary encoder to provide the step and the direction of the movement of an external device. Three axes (X, Y, Z) are supported. The integrated quadrature decoder can automatically decode the signals for the X, Y and Z axes of a HID input device, reporting step count and direction: the channels are expected to provide a pulse train with 90 degrees phase difference; depending on whether the reference channel is leading or lagging, the direction can be determined. This block can be used for waking up the chip as soon as there is any kind of movement from the external device connected to it.

10. Keyboard Controller

The keyboard controller can be used for debouncing the incoming GPIO signals when implementing a keyboard scanning engine. It generates an interrupt to the CPU.
Features:

- Generates a keyboard interrupt on key press or key release
- Implements debouncing time up to 31 ms

11. ADC

BR1002 is equipped with a high-speed low power 12-bit general purpose Analog-to-Digital Converter (GPADC). It can operate in unipolar (single ended) mode as well as in bipolar (differential) mode.
The ADC has its own voltage regulator (LDO) of 1.0V, which represents the full scale reference voltage.
Features：

- 12-bit dynamic ADC with 1 uS conversion time
- Maximum sampling rate 1M sample/s
- Single-ended as well as differential input with two input scales
- Single-ended or differential external input channels
- 6 single-ended or three differential external input channels
- Battery monitoring function
- Chopper function
- Offset and zero scale adjust
- Common-mode input level adjust

12. AUDIO ADC

The BR1002 has an audio PGA and ADC inside. The structure is as shown below; the PGA has a single input, which can be switched from MICN and MICP. The PGA gain varies from PGA GAIN -3 to +30db (3db step). The ADC gain varies from -6 to 12db (6db step).The PGA cascades ADC，dynamic range is 95dB, SNDR is 88dB, and SNR is 93 db.

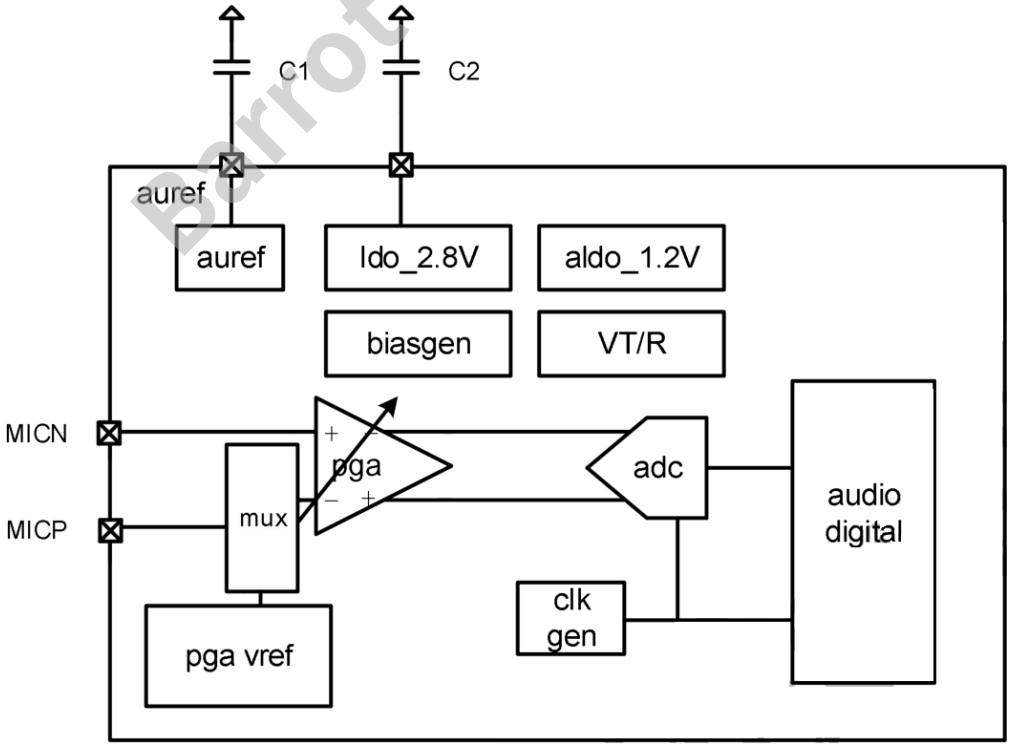

Figure 6 BR1002 audio PGA and ADC structure

13. Touch sensor controller

Capacitive touch sensors are user-interface devices that use the capacitance of the human body to detect the presence of a finger on, or near, a sensor. Capacitive sensors are aesthetically superior, easy-to-use, and have long lifetimes. BR1002 touch sensor controller offers excellent signal-to-noise ratio (SNR) and liquid tolerance, compatible with a wide variety of sensors such as buttons, sliders, and proximity sensors. The controller supports up to 16 capacitive sensing inputs, and a wide range of parasitic capacitor from 5 to 50pF.

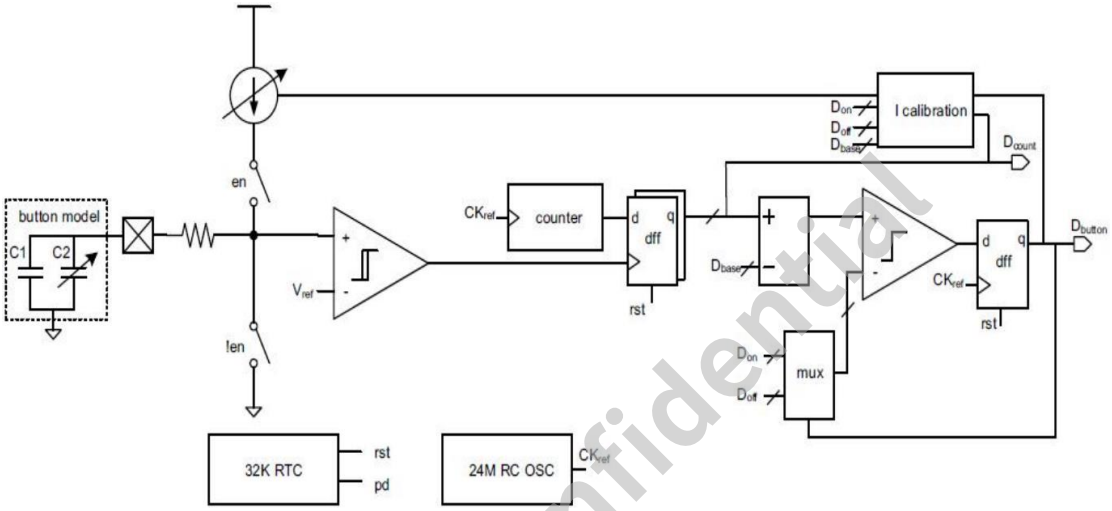

Figure 7 BR1002 Touch sensor controller structure

14. Power Management

BR1002 integrates a Power Management Unit (PMU).

14.1. Power Management Unit

There are four different power modes in the BR1002:

- Active Mode: System is active and operates at full speed.
- Sleep Mode: No power gating has been programmed; the CPU is idle, waiting for an interrupt. 32M crystal is on, 32K crystal is on. Peripherals is depending on the programmed enabled value.
- Deep Sleep Mode: All power domains are off except for the always on power domain, the programmed Bluetooth timer module, 32M crystal is off, and 32K crystal is on. The data retention SRAM retains its data and other SRAM is power off. It is wake by timer or GPIOs.
- Hibernation Sleep Mode: All power domains are off except for the hibernation power domain, and Bluetooth timer is off. This mode dissipates the minimum leakage power. It is wake by hibernation timer or GOIOs in this mode.

15. Bluetooth Low Energy Stack

15.1. Protocol Stack

BR1002 Software platform integrated Bluelet ® which is a qualified Bluetooth stack and BQB certification is QDID 77916. Bluelet ® supports almost Bluetooth profiles for consumer wellness, sport, fitness, and security and proximity applications are supplied as standard, while additional customer profiles can be developed and added as needed.

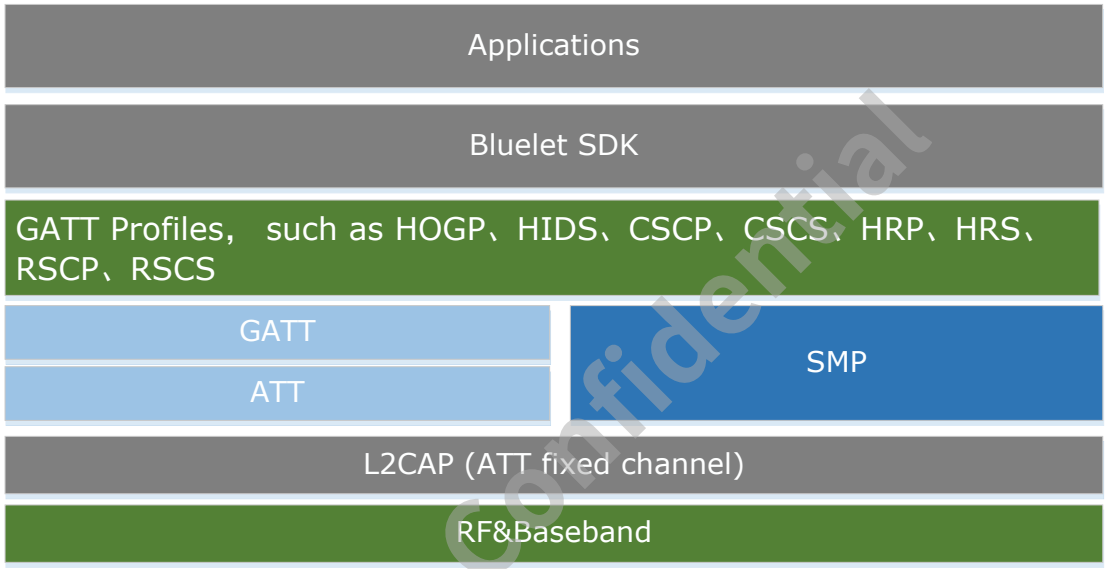

Figure 8 Bluelet ® Stack

Besides stack, software platform supports Hardware Abstraction Layer (HAL). Which allows it to easily access peripherals as shown in Figure below. BARROT provides a core driver for each interface of the BR1002. This optimizes the use of hardware features. Those drivers provide easy-to-use interface for hardware, so it is not necessary to do register-oriented programming. In spite of core drivers, In addition to the core drivers, BRT also provides many sample drivers which can communicate with Bluetooth application components, such as accelerometer, FLASH/EEPROM nonvolatile memory and etc.

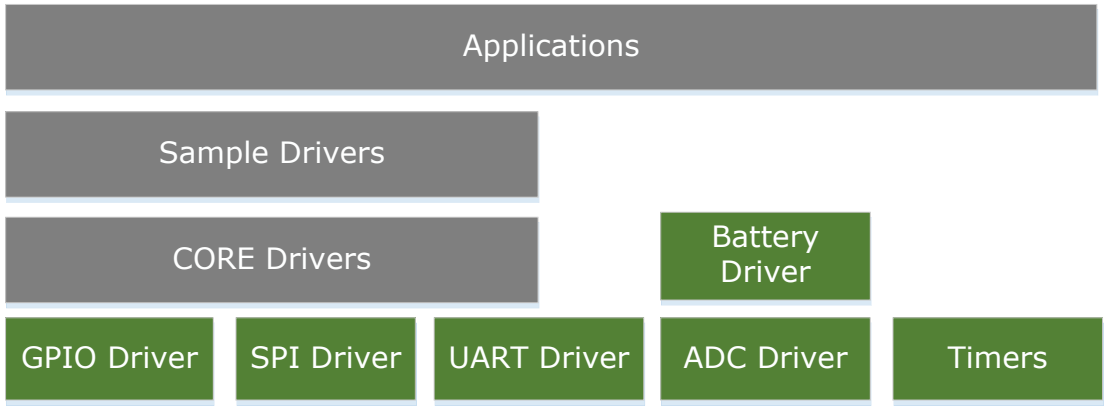

Figure 9 Peripherals Access

16. Package Information

The BR1002 has QFN32 package, the information is as below:

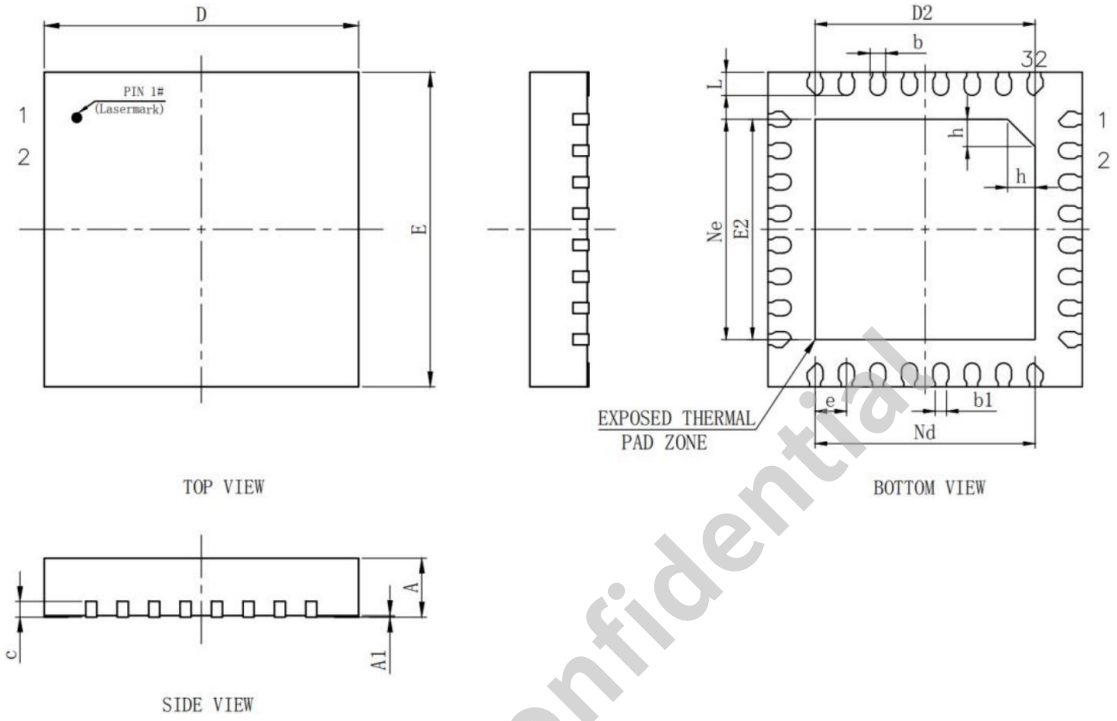

Figure 10 Package

Table 7 Package information

Symbol	Millimeter		
	Min	Nom	Max
A	0.80	0.85	0.90
A1	0	0.02	0.05
b	0.15	0.20	0.25
b1	0.14REF		
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	2.70	2.80	2.90
e	0.40BSC		
Ne	2.80BSC		
Nd	2.80BSC		
E	3.90	4.00	4.10
E2	2.70	2.80	2.90
L	0.25	0.30	0.35
h	0.30	0.35	0.40
L/F	122*122		

17. Application circuit

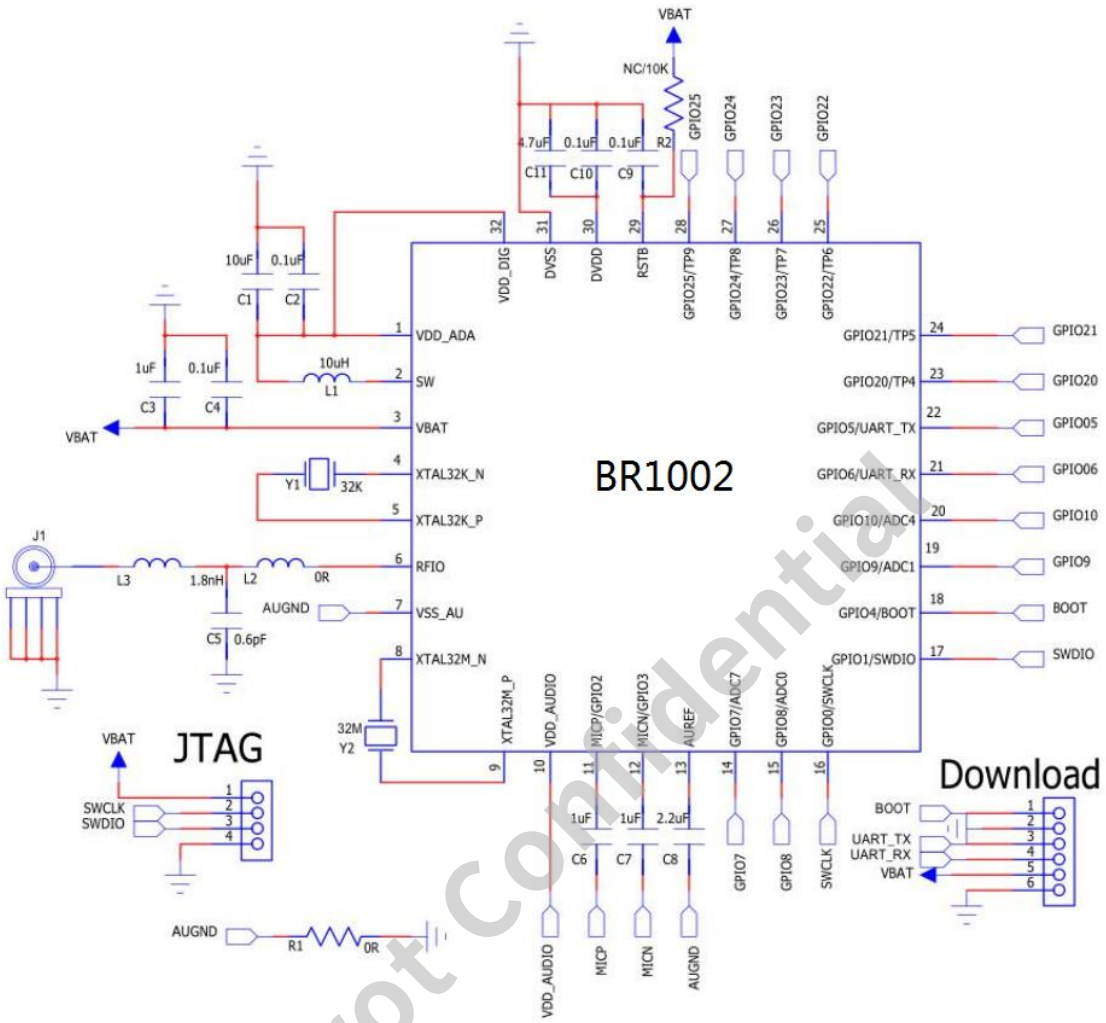

Figure 11 application circuit

18. Company Profile

Barrot Technology – Barrot is a world leading one-stop chipset level solution provider who offers wireless connectivity and audio intelligent hardware solutions featuring with own IPs. The company is an associated member of The Bluetooth SIG, and it is the only one who contributes to Bluetooth specification definition in China. Barrot owns three high-tech IPs: Bluetooth RF, Bluetooth stack and Acoustic algorithms, so Barrot offers most integrated, robust, reliable, and easy-to-use wireless turn-key solutions for IOT, Automotive and Wireless audio applications.

Barrot devotes itself to being the most reliable short distance wireless technologies' solution provider in the world.

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