BARROT

BR1001 Datasheet

September 20, 2019

Version 1.3

Version History

REVISION	AMENDMENT	DATE	AUTHOR
1.0	Initial version	2019-04-08	BaoQiang.Huang
1.1	Add Software information Delete application, refer separate document	2019-06-21	YongQiang.Xu
1.2	Update the spi connection and interface timing diagrams Update the baseband diagram Update Power Consumption	2019-07-09	Joe YongQiang.Xu
1.3	Update Bluetooth Version5.0	2019-09-20	KaiYue.wu

Contents

Description

BR1001 is a customized system on-chip (SOC) for 2.4G Bluetooth Low Energy (BLE) wireless MCU application. It includes a 2.4GHz ISM band RF Transceiver as wireless connection. Also it contains a single low power RISC 32-bits CPU inside, which is for run wireless stack and support MCU role. It is targeted a compact, low cost, low power and high performance wireless MCU. Compatible for Bluetooth V5.0 core spec.

Processor

- ARM CM3, max 48MHz
- Dedicated Link Layer Processor
- Supports Over-The-Air Upgrade (OTA)
- JTAG software upgrade
- ROM start
- Support debug mode

Power Management

- Multiple power management modes. Support software shutdown and hardware wake-up (by all GPIOs or WAKE PIN)
- Down to 5uA current consumption with deep sleep mode
- Support self-charging

Memory

- 128KB SRAM
- 256KB ROM，ROM encryption
- 4Mb sflash

Digital controlled oscillators

- 32.768K crystal oscillator clock, 32.768K RC clock
- 24M crystal oscillator clock, 24M RC clock

Digital interfaces

- 3 x general 32bit timer （Each timer has 4 routes）
- 31 GPIO. 2/5/10/20mAdriving capability. Internal pull-up, pull-down or open-circuit(adjustable resistor, strong/weak pull-up/pull-down). Analog input. Digital input/output. All GPIOs supports high\low voltage interruption.
- 2 x SPI interface
- 1 x I2C interface
- 2 x UART interface
- Keyboard control, 8X18
- QDEC (3 routes）
- Battery detection
- Watch dog & RTC
- 8 x 12bit ADC
- 4 channel DMA

Hardware Security

- AES-128 Security Module
- Random Number Generator (RNG)

Radio Transceiver

- Fully integrated 2.4 GHz CMOS transceiver
- Single wire antenna: no RF matching or RX/TX switching required
- Single Supply Current at VBAT, 2.0Vto 3.6V
- Programmable Output Power up to +2 dBm, 24dB PA dynamic range
- RX sensitivity: < -93dBm
- Low power RF: 10mApeak RX, 10mA peak TX (0dBm)
- Build in RSSI function

Package:

- QFN-48, 6x6*0.75mm, pitch 0.4mm

Application

- Support Bluetooth low energy V5.0 stack
- Support 6LoWPAN
- Home and Building Automation
- Connected Appliances, Lighting, Locks, Gateways, Security Systems
- Industrial
- Logistics, Production and Manufacturing, Automation, Asset Tracking and Management, Remote Display, Cable Replacement, HMI, Access Control
- Retail
- Beacons, Advertising, ESL and Price Tags, Point of Sales and Payment Systems
- Health and Medical
- Thermometers, Blood Glucose and Pressure Meters, Weight Scales, Vitals Monitoring, Hearing Aids
- Sports and Fitness
- Activity Monitors and Fitness Trackers, Heart Rate Monitors, Running Sensors, Biking Sensors, Sports Watches, Gym Equipment, Team Sports Equipment
- GATT and HID over GATT
- Remote Controls, Keyboards and Mice, Gaming
- Accessories
- Toys, Trackers, Luggage Tags, Wearables

Figure 1 IC

1. Block Diagram

BR1001 supports user secondary development and provides a simpler interface. it integrates Bluetooth baseband, PHY and 2.4GHz dual-way data communication protocol and profiles (GATT master and slave, HID over GATT). BR1001 can exchange data access system hardware resources through AHB bus, and all other peripherals access APB bridge and APB bus through AHB.

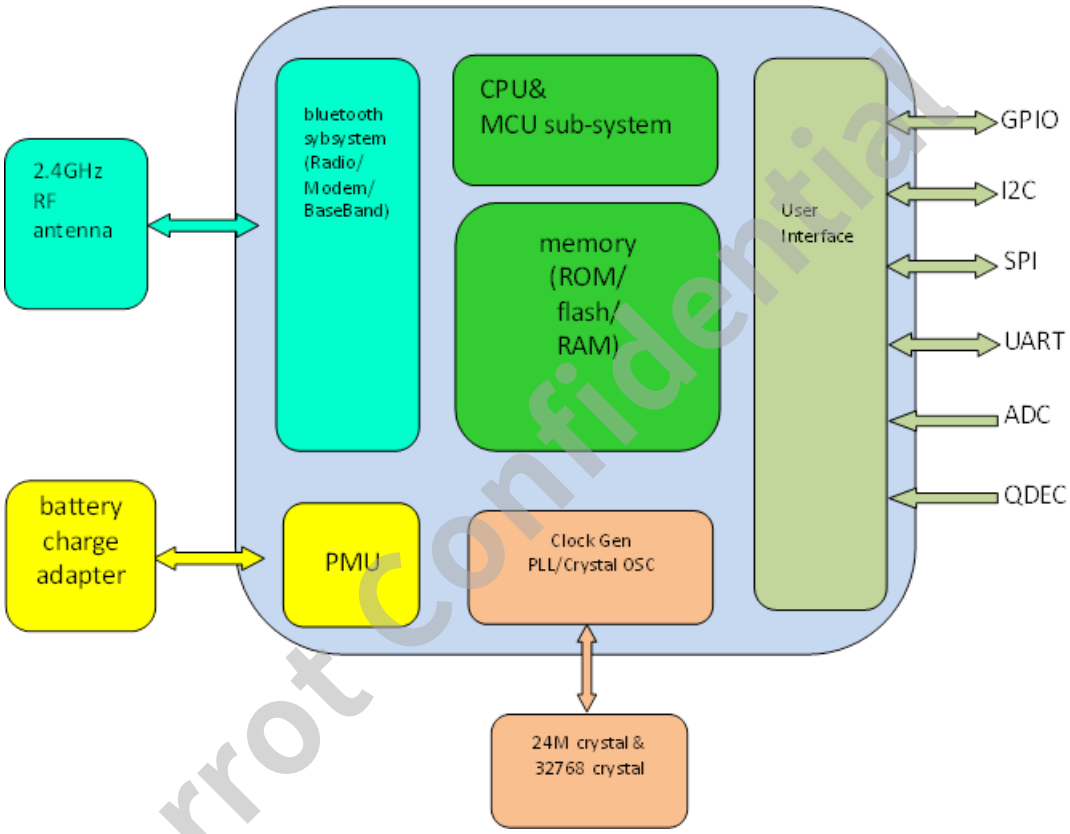


Figure 2 BR1001 Functional Diagram

2. PIN Description

2.1. PIN Diagram

BR1001's size is 6mm*6mm*0.75mm QFN48 package. Figure 2 shows the QFN48 pin definition. BR1001 have GND PAD in the center.

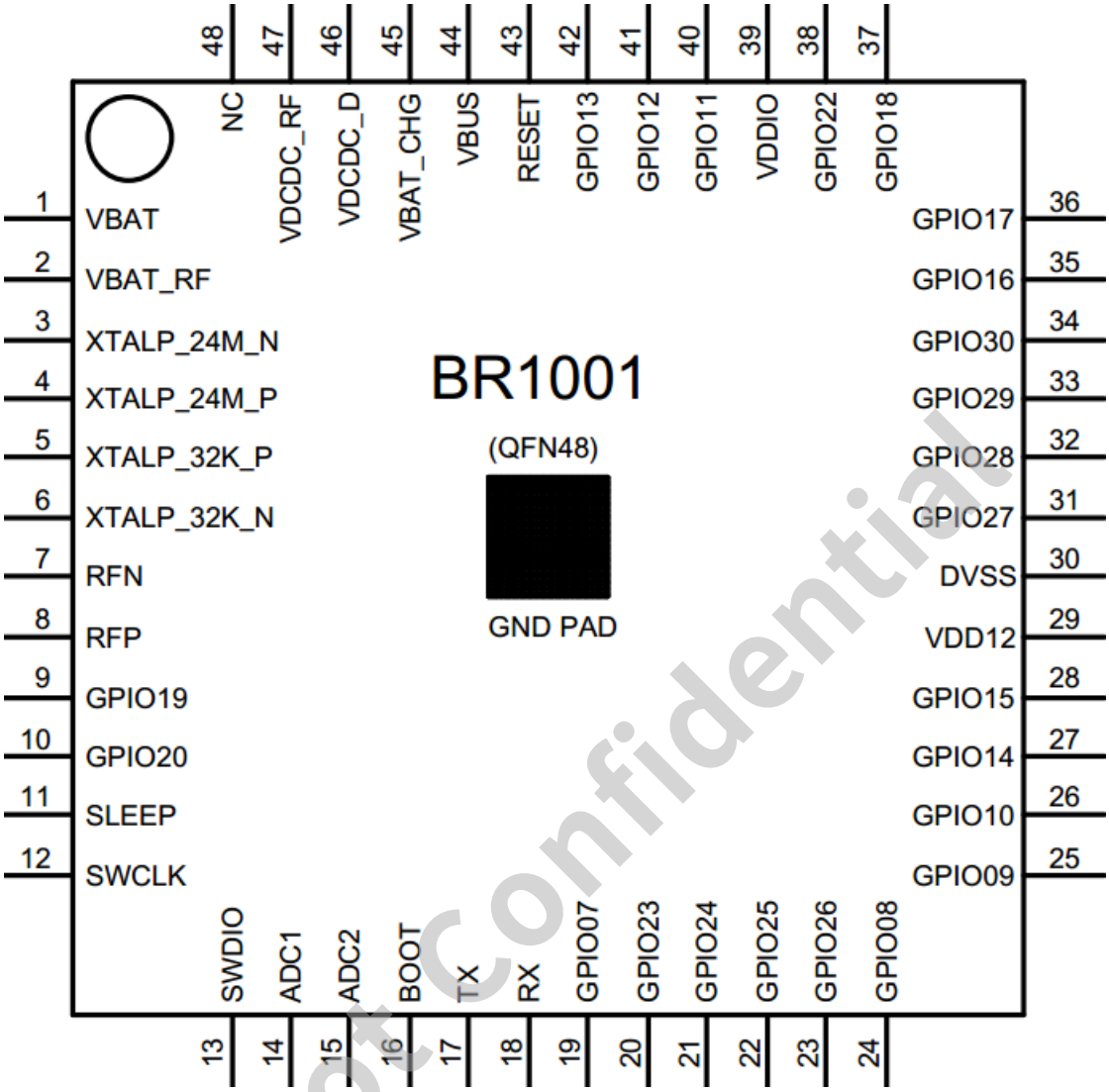


Figure 3 PIN

2.2. PIN Definition

Table 1： PIN Definition

No.	Name	Type	Description	Comments
1	VBAT	VDD	Battery voltage input	-
2	VBAT_RF	Power	Connect to VBAT	-
3	XTALP_24M_N	Analog	24MHz crystal output	-
4	XTALP_24M_P	Analog	24MHz crystal input	-

5	XTALP_32K_P	Analog	32.768KHz crystal input	-
6	XTALP_32K_N	Analog	32.768KHz crystal output	-
7	RFN	Analog	RF Ground	-
8	RFP	Analog	RF input/output	-
9	GPIO19	Digital	Digital GPIO	Configurable I/O
10	GPIO20	Digital	Digital GPIO	Configurable I/O
11	SLEEP	Digital	High effective	fixed I/O
12	SWCLK	Digital /Analog	Digital GPIO/ADC input/JTAG_CLK	Configurable I/O
13	SWDIO	Digital /Analog	Digital GPIO/ADC input /JTAG_DATA	Configurable I/O
14	ADC1	Digital /Analog	Digital GPIO/ADC input	Configurable I/O
15	ADC2	Digital /Analog	Digital GPIO/ADC input	Configurable I/O
16	BOOT	Digital	Programming Low effective	fixed I/O
17	TX	Digital	UART send	fixed I/O
18	RX	Digital	UART receive	fixed I/O
19	GPIO07	Digital /Analog	Digital GPIO/ADC input	Configurable I/O
20	GPIO23	Digital	Digital GPIO	Configurable I/O
21	GPIO24	Digital	Digital GPIO	Configurable I/O

22	GPIO25	Digital	Digital GPIO	Configurable I/O
23	GPIO26	Digital	Digital GPIO	Configurable I/O
24	GPIO08	Digital	Digital GPIO	Configurable I/O
25	GPIO09	Digital	Digital GPIO	Configurable I/O
26	GPIO10	Digital	Digital GPIO	Configurable I/O
27	GPIO14	Digital	Digital GPIO	Configurable I/O
28	GPIO15	Digital	Digital GPIO	Configurable I/O
29	VDD12	Power	Digital power supply	-
30	DVSS	Ground	Digital Ground	-
31	GPIO27	Digital	Digital GPIO	Configurable I/O
32	GPIO28	Digital	Digital GPIO	Configurable I/O
33	GPIO29	Digital	Digital GPIO	Configurable I/O
34	GPIO30	Digital	Digital GPIO	Configurable I/O
35	GPIO16	Digital	Digital GPIO	Configurable I/O
36	GPIO17	Digital	Digital GPIO	Configurable I/O
37	GPIO18	Digital	Digital GPIO	Configurable I/O
38	GPIO22	Digital	Digital GPIO	Configurable I/O
39	VDDIO	Power	Digital IO power supply	-
40	GPIO11	Digital	Digital GPIO	Configurable I/O
41	GPIO12	Digital	Digital GPIO	Configurable I/O
42	GPIO13	Digital	Digital GPIO	Configurable I/O

43	RESET	Digital	Reset	Active low Pull-up when not used
44	VBUS	Power	USB power supply	-
45	VBAT_CHG	Power	Battery power supply	-
46	VDCDC_D	Power	LDO supply output	-
47	VDCDC_RF	Power	Connect to VDCDC_D	-
48	NC	NC	NC	-

3. Electrical Characteristics

3.1. Absolute Maximum Ratings

Table 2：Absolute Maximum Ratings

Rating	Mode	Min	Max	Unit
Storage temp.	-	-40	120	°C
ESD (Electro-Static Discharge)	Human Body Mode	2000	-	V
	Machine Mode	200	-	V
	Charge Device Mode	500	-	V

3.2. Recommended Operating Conditions

Table 3：Recommended Operating Conditions

Rating	Min	Typ.	Max	Unit
Operating temp.	-40	-	85	°C
Digital supply voltage	0.95	1.05	1.2	V

RF supply voltage	1.4	1.5	1.6	V
I/O supply (Vsupply>3.3)	3.1	3.3	3.5	V
I/O supply (Vsupply<3.3)	Vsupply	Vsupply	Vsupply	V
Power supply	2.0	3.3	3.6	V

3.3. Battery Charging

Table 4 Battery Charging

Charge modes	**Min**	**Typ.**	**Max**	**Unit**
Charging voltage (V IN)	-	5	-	V
Battery trickle charging current	-	35	-	mA
Max battery charging current	-	300	-	mA
Battery trickle charging voltage threshold	-	2.9	-	V
Percentage of battery end-of-charge current and fast charging current	-	10	-	%

3.4. BLE RF Characteristics

3.4.1. Transmitter

Table 5：RF Transmitter Characteristics

Parameters	**Min**	**Typ.**	**Max**	**BLE Standards**	**Unit**
Max RF transmit power	-	2	-		dBm
RF transmit power	-18	-	2	-	dB

Frequency offset	-	4.02	-	-150~150	KHz
Frequency drift	-	-3.31	-	-50~50	V
Frequency drift rate	-	-3.13	-	-20~20	KHz/50us
Initial Frequency drift	-	-2.25	-	-20~20	KHz
Modulation Δf 1avg	225	250	275	-	KHz
Modulation Δf 2max	100%	-	-	>99.9%	-
Modulation Δf 2avg /Δf 1avg	0.84	-	-	>0.8	-

3.4.2. BLE Receiver

Table 6：BLE Receiver

Parameters	**-**	**Min**	**Typ.**	**Max**	**BLE Standards**	**Unit**
Sensitivity--PSR9 37byte package	-	-93	-90	-81	≤-70	dBm
Max receive signal	-	-	10	-	0	dBm
In-band interference --I/C value	-	-		9	-21	dB
Out-of band-interference --I/C value （F0=2440MHz）	F = F 0 +1MHz	-	-	1	-15	dB
	F = F 0 -1MHz	-	-	-3	-15	dB
	F = F 0 +2MHz	-	-	21	15	dB
	F = F 0	-	-	23	15	dB

	-2MHz					
	F = F 0 +3MHz	-	-	33	27	dB
	F = F 0 -3MHz	-	-	34	27	dB

3.5. Power Consumption

Table 7: Chipset Power Consumption(with Ext DCDC, VBAT=3.3V, 25°C, 2dBm output power)

Operation Modes		**Min**	**Typ.**	**Max**	**Unit**
Deep sleep		1.1	14.6	18	uA
Advertising, discoverable (1.28S advertising interval)		16.0	80.5	9300	uA
Scanning (1.28s scan interval, 11.25ms scan window)		16.8	267	9300	uA
Connected (500ms conn interval Empty TX and RX LL packets)	Master role	12.8	128	7800	uA
	Slave role	12.6	147	1190	uA

4. Functions Description

4.1. RF Transmitter

The Radio Transceiver implements the RF part of the Bluetooth Low Energy protocol. Together with the Bluetooth 5.0 PHY layer, this provides a reliable wireless communication. All RF blocks are supplied by on-chip low-drop out-regulators (LDO's). The Bluetooth LE radio comprises the Receiver, Transmitter, Synthesizer, Rx/Tx
combiner block, and Biasing LDO's.

4.2. Bluetooth Baseband Unit

The BR1001's BLE core is a qualified Bluetooth V5.0 baseband control unit which is compliant with Bluetooth smart specification. The BLE core is used to data block encoding/decoding and frame scheduling. The features are as follows:

- Support all device class（broadcaster, central, observer, peripheral）
- All data package type(Advertising / Data / Control)
- Encryption（AES-128）
- Bit stream processing（CRC）
- Frequency modulation calculation
- Low power mode supports 32.768kHz

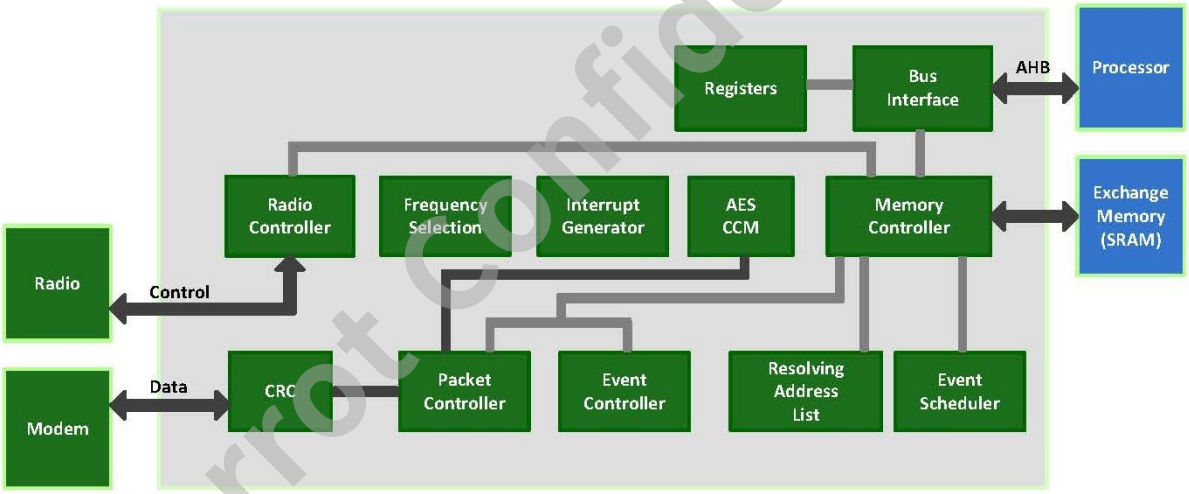


Figure 4 BR1001 Baseband

5.Interfaces Description

5.1. SPI

The Serial Peripheral Interface (SPI) bus is a synchronous serial communication interface specification used for short distance communication, primarily in embedded systems. The BR1001 integrate 2 SPI interfaces, they can work in either master or slave mode and also support DMA or software mode to transfer data.

The master or slave controller only support point to point connection by

hardware, that is, both the SPI interface has only one CS pin. The connection is shown below the figure:

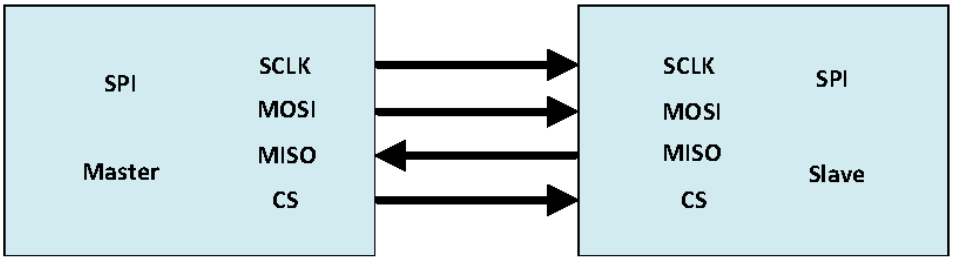


Figure 5 SPI Connection

The flexibility of SPI interface makes it suitable for most of SPI slave devices. SPI offers four modes due to the programmable ability of SCK's polarity and phase. The delay from CS to SCK, the delay from SCK to NCS and SCK period are also programmable. SPI interface timing diagram is shown in Figure5 below.

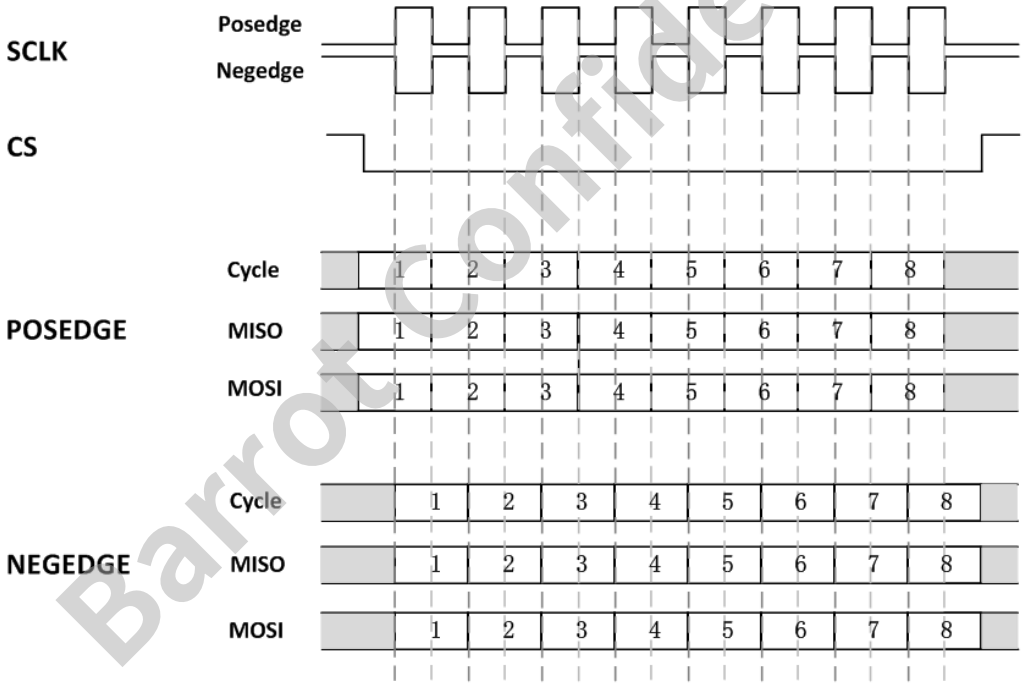


Figure 6 SPI Interface Timing Diagram

5.2. UART

The UART is used for serial communication with a peripheral, modem (data carrier equipment, DCE) or data set. Data is written from a master (CPU) over the APB bus to the UART and it is converted to serial form and transmitted to the destination device. Serial data is also received by the UART and stored for the master (CPU) to read back. The UART contains registers to control the character length, baud rate, parity generation/checking, and interrupt generation. Although there is only

one interrupt output signal from the UART, there are several prioritized interrupt types that can be responsible for its assertion. Each of the interrupt types can be separately enabled or disabled by the control registers.
BR1001 has 2 UART; the UART0 is a common 2 wire (transmitter and receiver) controller, and the UART1 support stream control (CTS/RTS). UART1 also supports ISO7816 protocols.

5.3. I2C

The I2C is a master or slave interface. It supports 100, 400 and 800 KHz clock rates for controlling EEPROM and etc. The I2C interface provides several data formats and can fit various I2C peripherals. Sequential read and write are supported to improve throughputs. The I2C support DMA operation for extra MCU free data transfer. The I2C work as either master or slave, but cannot change the working mode after configuration.

6. Timers

Timer includes three same 32bit timer/counter channels. Each channel is programmable to execute frequency measurement, events counting, interval measurement, pulse generation, latency, and pulse width modulation. Each channel drives an internal interrupt signal which can be programmable to generate processor interrupt.

7. GPIO

BR1001 offers 31 programmable GPIOs featuring with

- Programmable GPIOs;
- Each I/O can choose either pull-up or pull-down resistors;
- GPIO [7:0] can be configured to GP-ADC input;
- Each I/O remains the last state when the chipset enters sleep mode;
- Each I/O interrupt can wake up chipset from sleep mode.

8. I2S

I2S consists of three lines: serial data, word select, and serial clock. I2S interface is used for audio data communication. BR1001 I2S supports master/slave mode, and

this interface is only used for data transmit. I2S interface supports standard I2S frame format.

9. ADC

BR1001 integrates high speed and low power consumption 12-bit General Purpose Analog-to-Digital Converter(GPADC) for sampling an external signal. It can operate in unipolar (single-ended) mode as well as bipolar (differential) mode. The ADC has its own 1.2V voltage regulator (LDO), which represents the full-scale reference voltage.

Features：

- 12-bit dynamic ADC with 65 ns conversion time
- Maximum sampling rate 3.3M sample/s
- Ultra-low power (5 μA typical supply current at 100k sample/s)
- Single-ended as well as differential input with two input scales
- Eight single-ended or four differential external input channels
- Battery monitor function
- Chopper function
- Offset and zero scale adjustment
- Common-mode input voltage adjustment

10. Power Management

BR1001 integrates Power Management Unit (PMU) and battery charging unit.

10.1. Power Management Unit

BR1001 has four power modes:

- Active Mode: system is fully active and running at full speed.
- Sleep Mode: No power gating has been programmed; the CPU is idle, waiting for an interrupt. 24M crystal is on, 32K crystal is on. Peripherals are depending on the programmed enabled value.
- Extended Sleep Mode: All power domains are off except for the always-on power domain, the programmed Bluetooth timer module, 24M crystal is off, 32K crystal

is on. The data retention SRAM retains its data and other SRAM is power off. It is wake by timer or GPIOs

- Deep Sleep Mode: All power domains are off except for the always on power domain, and all clocks are off. This mode dissipates the minimum leakage power. It is wake only by GOIOs in this mode.

10.2. Battery Charging Unit

When the charging circuit is enabled , it will detect the battery voltage and enter the relevant mode to charge the battery, which is Trickle, CC or CV mode. When the battery voltage reaches a high threshold, the charger will enter standby mode and continuously monitor the battery voltage. If the battery voltage drops to a lower threshold, the charger circuit will again charge the battery.

10.3. Power sequence:

normal work mode:

Figure 7 power sequence 1

Program mode：

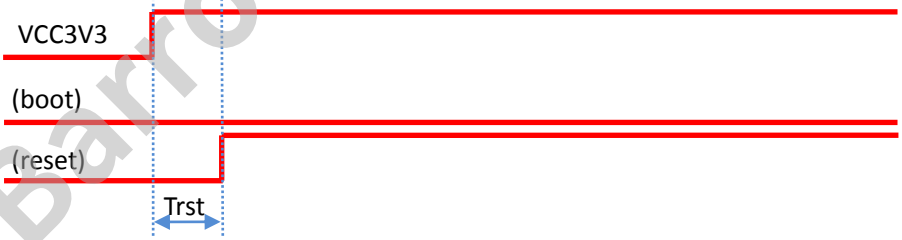


Figure 8 power sequence 2

Trst：>50mS

11. Bluetooth Low Energy Stack

11.1. Protocol Stack

BR1001 Software platform integrated Bluelet ® which is a qualified Bluetooth stack

and BQB certification is QDID 77916. Bluelet ® supports almost Bluetooth profiles for consumer wellness, sport, fitness, and security and proximity applications are supplied as standard, while additional customer profiles can be developed and added as needed.

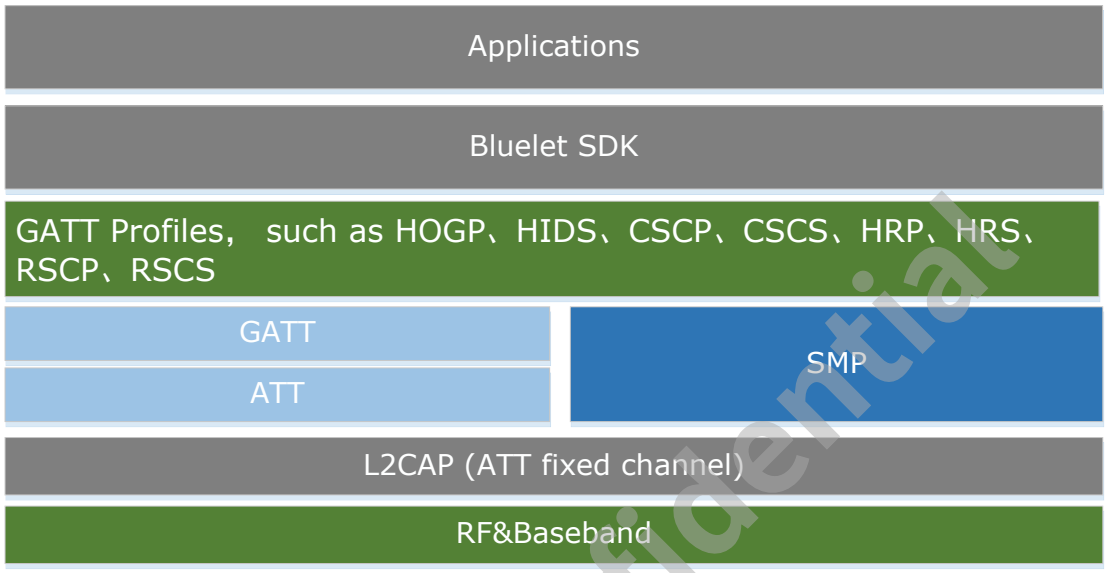


Figure 9 Bluelet ® Stack

Besides stack, software platform supports Hardware Abstraction Layer(HAL). which allows it to easily access peripherals as shown in Figure 7 below. Barrot provides a core driver for each interface of the BR1001. This optimizes the use of hardware features. Those drivers provide easy-to-use interface for hardware, so it is not necessary to do register-oriented programming. In spite of core drivers, In addition to the core drivers, BRT also provides many sample drivers which can communicate with Bluetooth application components, such as accelerometer, FLASH/EEPROM nonvolatile memory and etc.

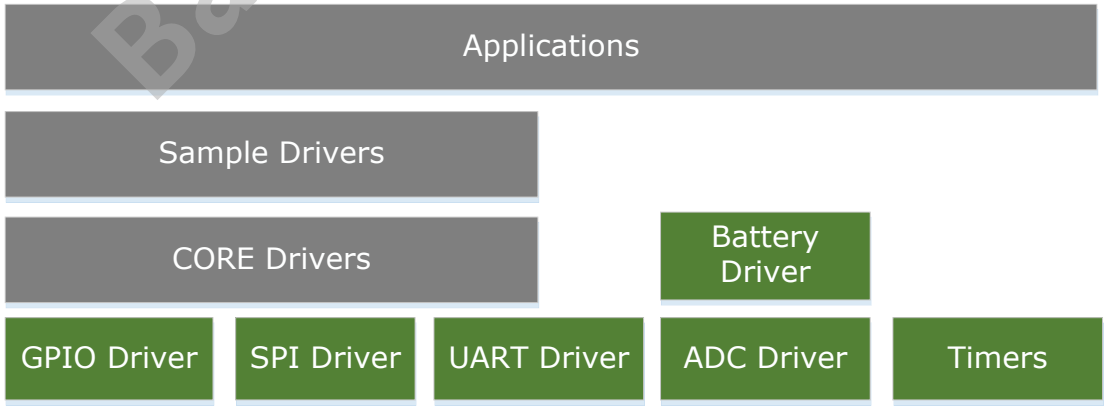
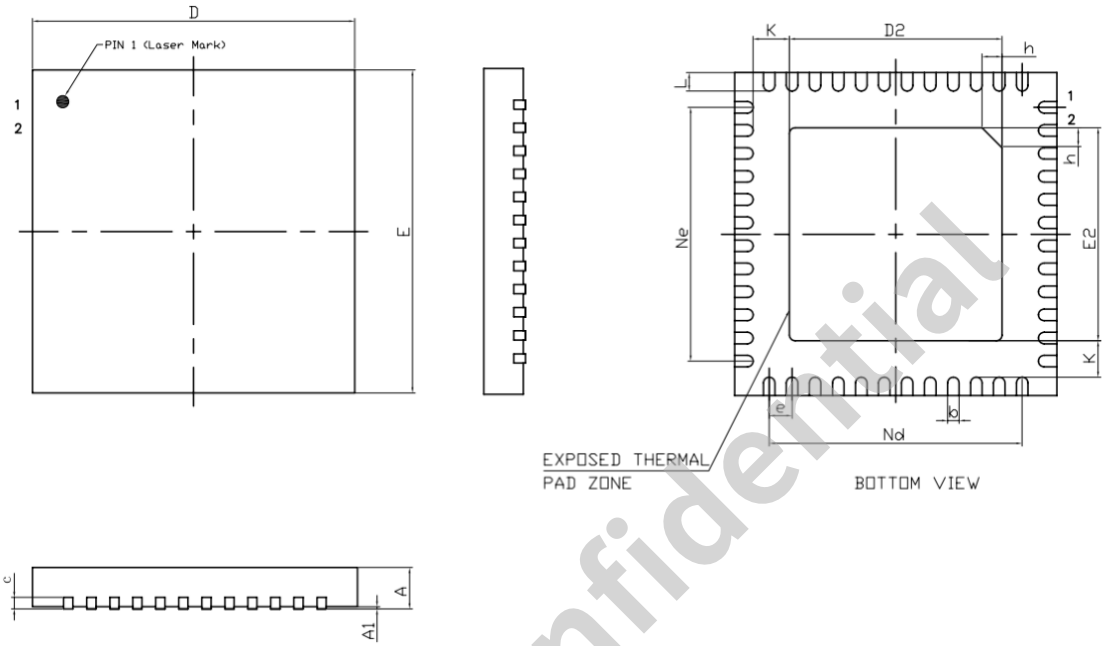


Figure 10 Bluelet ® Stack

12. Package Information

BR1001 is QFN48 package. Figure 8 shows package information.



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.23
D	5.90	6.00	6.10
D2	3.70	3.80	3.90
e	0.40BSC		
Ne	4.40BSC		
Nd	4.40BSC		
E	5.90	6.00	6.10
E2	3.70	3.80	3.90
K	0.20	--	--
L	0.35	0.40	0.45
h	0.30	0.35	0.40
L/F载体尺寸 (MIL)	161*161		

Figure 11 Package information

13. MOQ

Package： Reel
The minimum number of packages: 3000pcs/ Reel

14. Company Profile

Barrot Technology – Barrot is a world leading one-stop chipset level solution provider who offers wireless connectivity and audio intelligent hardware solutions featuring with own IPs. The company is an associated member of The Bluetooth SIG, and it is the only one who contributes to Bluetooth specification definition in China. Barrot owns three high-tech IPs: Bluetooth RF, Bluetooth stack and Acoustic algorithms, so Barrot offers most integrated, robust, reliable, and easy-to-use wireless turn-key solutions for IOT, Automotive and Wireless audio applications.

Barrot devotes itself to being the most reliable short distance wireless technologies' solution provider in the world.

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